In the Specification:

Please substitute the following paragraphs for the corresponding paragraphs beginning at the indicated location in the specification as originally filed.

Paragraph 0004:

~~SOI film transistors is to provide a raised source~~ A known technique for reducing resistance in thin SOI film transistors is to provide a raised source and drain (RSD) structure by growth of additional semiconductor material in the source and drain regions. However, RSD structures are generally formed adjacent a thin spacer on the sides of the transistor gate and increase the overlap capacitance (the capacitance between the extension impurity region and the gate electrode across the gate dielectric and thin spacer) significantly; degrading transistor performance. Typical capacitance increases for a 30 nm RSD are about 0.08fF/μm (about 25% increase) for a 10 nm oxide spacer and about 0.2 fF/μm (about 50% increase) for a 10 nm nitride spacer. Additionally, the minimal thickness of the spacer appropriate to reducing resistance through the use of RSD structures places the source/drain implants too close to the gate.

Paragraph 0019:

For example, if structure 12 is formed of an oxide or other insulator, a bulk semiconductor wafer can be effectively converted into a hybrid wafer having many of the beneficial properties generally associated with a silicon-on-insulator (SOI) wafer but with substantial cost savings and with the added advantages that the depth of structure 12 can be varied at will to define the thickness of the conduction channel of the transistor and floating body effects can be avoided. Further, the shaping of structure 12 may be readily controlled, for example, to form region 14 which may be

used to shape structure 12 in, for example, a "staircase" cross-sectional profile that can be used to emulate an UT-SOI wafer in regard to the confinement of channel depth with the additional advantage that a greater thickness of semiconductor material may be provided for source and drain structures that would not be available on a SOI or UT-SOI wafer. Further, the patterning of structure 12, which may be performed in a manner self-aligned with the gates, provides a further region 18 which can be used, for example, to provide a conduction path to the channel to prevent floating body effects, alluded to above, or other desired effects or structures such as a further gate to provide a dual-gate FET and/or to localize stresses applied from a stressed film which can enhance carrier mobility.

Paragraph 0025:

It should also be noted from Figure 5 that silicon is exposed at the sides of region 50. As shown in Figure 6, silicon may then be epitaxially grown thereon. Silicon will not be grown on the oxide covering the SiGe but growth starting from region 50 may extend over a portion thereof to form spacers 60. Further, epitaxial silicon growth occurs on the exposed silicon on the back surface of thin silicon layer 24 to form recessed extension and source and drain (E&SD) regions 62. Then, as shown in Figure 7, a further arsenic implant and annealing are optionally but preferably performed, followed by a selective (to undoped silicon) etching process to be certain of avoiding shorting of the grown silicon spacer and the recessed E&SD regions. Since the silicon is selectively grown from exposed silicon but not oxide, any grown silicon (e.g. 70) which might connect these regions will be thinner over the oxide and can be readily removed by etching (e.g. to profile 70' of Figure 8). Then, as shown in Figure 8 the void is

filled with deposited oxide; yielding a discontinuous oxide film having a cross-sectional shape similar to that of regions 12 of Figure 1 and an aperture ~~apertures~~ aligned with the gate structure of the transistor. This structure yields a transistor (when completed by self-aligned extension, source/drain and/or halo implants and contact formation by any known processes) with a well confined shallow channel and sharp lateral junction due to the confinement of impurity diffusion by the upper end 18 of oxide 52. At the same time, the thickness of the recessed E&SD 62 may be made substantially greater than the channel depth to reduce or limit resistance. An ohmic connection of controllable resistance to the channel region is also formed at the apertures in the insulating film to avoid floating body effects with an arbitrarily small effect on the transistor performance since the resistance of connection 18 can be made readily controlled by control of the dimensions of the connection.

Paragraph 0026:

Accordingly, it is seen that the invention provides for a structure of relatively arbitrary cross-sectional shape and materials to be developed within a layer of semiconductor material such as a bulk semiconductor wafer and which can impart useful and desirable characteristics to a transistor or other active device while potentially reducing the cost thereof. In the case of the first preferred embodiment described above, a recessed extension and source-drain structure allows a shallow channel such as might be obtained from a SOI wafer in a much less expensive layer or wafer of bulk silicon while obtaining the further advantages of reduced resistance and/or overlap capacitance and avoiding the floating body effects incident to SOI FET structures. Another, second group

of beneficial and desirable effects can be obtained in accordance with a second preferred embodiment of the invention which will now be discussed in connection with Figures 9 - ~~20~~ 19.